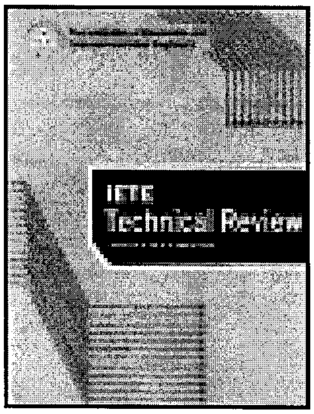

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CDCTA and OTA Realizations of a Multi-phase Sinusoidal Oscillator

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ABSTRACT

A new topology for a current-mode multi-phase sinusoidal oscillator (MSO) is introduced. It is designed using current-differencing cascaded transconductance amplifiers (CDCTAs) and operational transconductance amplifiers (OTA). Both designs realize odd and even numbers of phase oscillators. The MSO is implemented by cascading first-order all-pass filter stages that are designed with CDCTAs or OTAs and show the same transfer function. The MSO includes *n* grounded resistors and *n* grounded capacitors to generate *n* phases. We highlight the advantage of using OTAs because the resulting MSO circuitry is greatly reduced compared to using CDCTAs, while in both designs the high output impedances facilitate easy driving an external load without additional current buffers. The condition of oscillation and the frequency of oscillation are orthogonal and can be adjusted by varying a bias current. Finally, SPICE simulation results using integrated circuit technology of 0.35 μm show that the designed MSO provides odd/even phase signals that are equally spaced in phase and with equal amplitude.

***Keywords*:**
Current-mode, CDCTA, Integrated circuit, Multi-phase sinusoidal oscillator, OTA.

1. INTRODUCTION

Multi-phase sinusoidal oscillators (MSOs) are important building blocks used in applications like phase modulators and quadrature mixers. Traditionally, they were designed using voltage-mode topologies, but from two decades ago, analogue integrated circuit (IC) designers have shown the usefulness of using current-mode topologies, as shown by references [1–15]. In this manner, we introduce a new current-mode topology that is designed by using two kinds of active devices: current-differencing cascaded transconductance amplifiers (CDCTAs) and operational transconductance amplifiers (OTAs). We show that the OTA realization has reduced circuitry compared to using CDCTAs.

MSOs have been realized using different active devices, such as: current followers [1], current-controlled second-generation current conveyor (CCCII) [2,3], current-differencing transconductance amplifier (CDTA) [4–6], current-differencing buffer amplifier [7], current-feedback operational amplifier [8], current-controlled current conveyor transconductance amplifier [9], and current-controlled CDTA [10]. However, those MSO realizations have the following drawbacks: the design in [1] requires two current followers, one floating resistor, and one floating capacitor for each phase, and thus the topology is not suitable for IC design. The CCCII design in [2,3] provides high output impedances and electronic tunability but at the expenses of several external capacitors, and the condition of oscillation (CO) is tuned by the ratio of external capacitors or requires additional current amplifiers. The MSO designs in [4,5] are based on lossy integrators implemented with CDTAs; they consist of CDTA-based all-pass sections and exhibit good electronic tunability, high output impedances, and independent tuning of the CO and frequency of oscillation (FO). However, they require an additional current amplifier implemented by two CDTAs, and the output currents of the MSO have different amplitudes. The design in [6] also uses CDTA-based all-pass sections, but includes a floating capacitor that requires larger area for IC design [16]. The designs in [7–10] show either or both: disadvantages for IC implementation or large number of circuit elements for each phase signal.

To cope with the problems listed above, this article introduces a new current-mode MSO topology with the following main advantages:

- It uses grounded capacitors and identical circuit configuration for each phase signal.
- It provides orthogonal control of the CO and FO.

- It provides high output impedances and independent current outputs.
- It generates multi-phase signals (even and odd numbers) that are equally spaced and with equal amplitude.
- It requires only one CDCTA for each phase signal.
- A new reduced topology is introduced by cascading two three-output OTAs for each phase signal.

2. CDCTA MODEL

A CDCTA providing new possibilities in designing current-mode circuits was introduced in [11]. It is reviewed herein, and a new topology of a CDCTA-based all-pass filter is introduced in the next section. In addition, starting from the CDCTA design of the all-pass section, a new compact MSO realization is introduced by cascading all-pass sections that are designed by cascading two three-output OTAs.

The ideal behaviour of a CDCTA is described by Eq. (1), where g_{m1} and g_{m2} describe their transconductances and bias currents I_B can adjust them. All variables adding c are copies, for example: I_{zc} is a copy of I_z, and so on. Using bipolar junction transistors (BJTs), the transconductances are evaluated by Eqs. (2) and (3). The block description and the implementation of the CDCTA using controlled sources are shown in Figure 1. In both cases, Eq. (1) describes their behaviours.

$$\begin{bmatrix} I_z, I_{zc} \\ I_{x1}, I_{x1c} \\ I_{x2}, I_{x2c} \\ V_{x2} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & g_{m1} & 0 \\ 0 & 0 & 0 & g_{m2} \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_z \\ V_{x1} \end{bmatrix}, \tag{1}$$

$$g_{m1} = \frac{I_{B1}}{2V_T}, \tag{2}$$

$$g_{m2} = \frac{I_{B2}}{2V_T}. \tag{3}$$

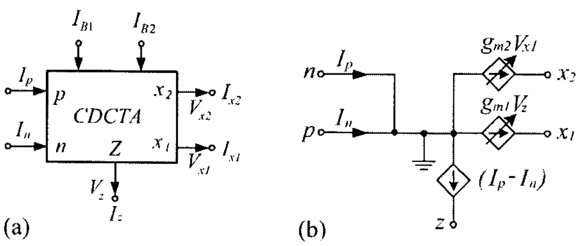

Figure 1: CDCTA: (a) block description and (b) equivalent circuit.

3. CASCADING FIRST-ORDER ALL-PASS SECTIONS

The MSO can be implemented by cascading at least two first-order all-pass sections. Figure 2 shows the generalized structure by cascading n identical stages ($n \geq 2$). This is an autonomous oscillator where the output of each nth stage is connected to the input of a first-order all-pass section. However, it is required that the output of the last section be inverted for implementing an even number of phases and non-inverted for implementing an odd number of phases. In this manner, the loop gain can be written as follows:

$$L(s) = -\left(k\frac{sa-1}{sa+1}\right)^n, \tag{4}$$

where k denotes the current gain and a denotes the natural frequency of each all-pass section. At the FO ω_{osc}, the Barkhausen's condition can be written by Eq. (5), from which the magnitude and phase are given by Eqs. (6) and (7), respectively.

$$L(j\omega_{osc}) = -\left(k\frac{j\omega_{osc}a-1}{j\omega_{osc}a+1}\right)^n = 1. \tag{5}$$

$$|L(j\omega_{osc})| = 1, \tag{6}$$

$$\angle H(j\omega_{osc}) = 2n\phi = 2n((-2\tan^{-1}(\omega_{osc}a)) = -2\pi. \tag{7}$$

Eq. (7) shows that for implementing an n-phase oscillator, each phase is shifted by $-360°/2n$. Hence the CO and FO are given by the following formulae:

$$\text{CO:}\quad k = 1, \tag{8}$$

$$\text{FO:}\ \omega_{osc} = \frac{1}{a}\tan\left(\frac{\pi}{2n}\right). \tag{9}$$

As one can infer, from Eqs. (8) and (9) it can be appreciated that the CO is controlled by the gain k, while the FO is tuned by the natural frequency a. In this manner, the MSO shown in Figure 2 is based on identical first-order all-pass sections, and our proposed CDCTA implementation is shown in Figure 3, including one grounded capacitor and one grounded resistor, thus suitable for IC design [16]. As mentioned in the previous section, all variables adding c are copies, in this case I_{zc} is a copy of I_z, and I_{-x1c} is a copy of I_{-x1}. By performing symbolic circuit analysis as in [17], the

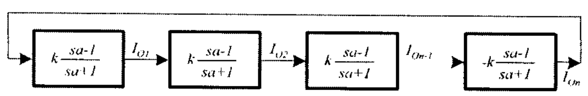

Figure 2: MSO block diagram for providing odd/even phases.

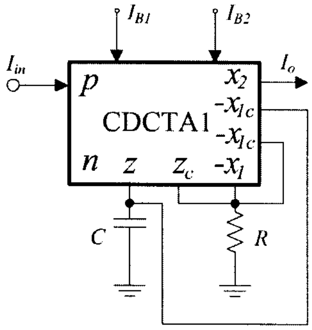

Figure 3: Proposed CDCTA-based all-pass filter topology.

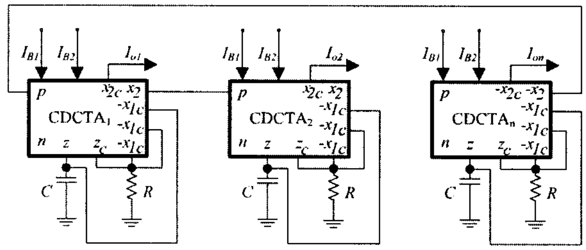

Figure 4: Proposed current-mode MSO for providing odd/even phases.

analytical expression for the current transfer function is given by Eq. (10). Also, by performing hand calculations: $I_o = -g_{m2}V_{x1}$, $V_{x1} = (I_{zc} - I_{x1} - I_{x1c})R$, $I_{x1} = g_{m1}V_z$, and $V_z = (I_z - I_{x1c})/sC$. Since $I_z = I_{in}$, $I_{x1c} = I_{x1}$, and $I_{zc} = I_z$, then: $I_o = -g_{m2}R(I_{in} - 2g_{m1}V_z)$ and $V_z = I_{in}/(sC + g_{m1})$. After algebraic manipulations one gets Eq. (10), where $L(s) = I_o/I_{in}$ and from which the CO and FO are given by Eqs. (11) and (12), respectively.

$$L(s) = -\left(g_{m2}R\frac{s\frac{C}{g_{m1}} - 1}{s\frac{C}{g_{m1}} + 1}\right)^n. \tag{10}$$

$$\mathrm{CO}: g_{m2}R = 1, \tag{11}$$

$$\mathrm{FO}: \omega_{osc} = \frac{g_{m1}}{C}\tan\left(\frac{\pi}{2n}\right). \tag{12}$$

Using BJTs, if $g_{m1} = I_{B1}/2V_T$ and $g_{m2} = I_{B2}/2V_T$, the CO and FO are described by Eqs. (13) and (14), respectively. Now, the CO and FO are adjusted independently by varying I_{B2} and I_{B1}, respectively.

$$\mathrm{CO}: \frac{I_{B2}R}{2V_T} = 1, \tag{13}$$

$$\mathrm{FO}: \omega_{osc} = \frac{I_{B1}}{2V_TC}\tan\left(\frac{\pi}{2n}\right). \tag{14}$$

4. CDCTA AND OTA REALIZATIONS

The MSO realization using our proposed all-pass filter from Figure 3 is shown in Figure 4. This topology provides odd and/or even number of phases, according to the number of all-pass sections. It is worth mentioning that current mirrors (CMs) are required to split the bias currents I_{B1} and I_{B2} to each all-pass section. In addition, the proposed current-mode MSO provides high output impedances facilitating easy driving of an external load without additional current buffers.

Using bipolar technology, the current-mode MSO is designed with PNP and NPN transistors using the parameters of the PR200N and NR200N of ALA400 transistor array from AT&T [12]. The structure of the CDCTA is shown in Figure 5 [13], which is biased with ±2.5 V; and $I_{B1} = 100$ μA, $I_{B2} = 62$ μA, C = 0.1 nF, and $R = 1$ kΩ.

In Figure 5, one can identify the CDCTA inputs p and n. However, the input n is not used, thus according to Eq. (1): the input p is processed through a dual-output current mirror (DO-CM) to provide the required terminals z and z_c. The first OTA embedding g_{m1} has two outputs to provide I_{x1} and I_{x1c} by processing the voltage generated at V_z. The second OTA embedding g_{m2} provides I_{x2} and I_{x2c} by processing the voltage generated at V_{x1}. This CDCTA shown in Figure 5 has been applied in [14], and in this article it is only used as a

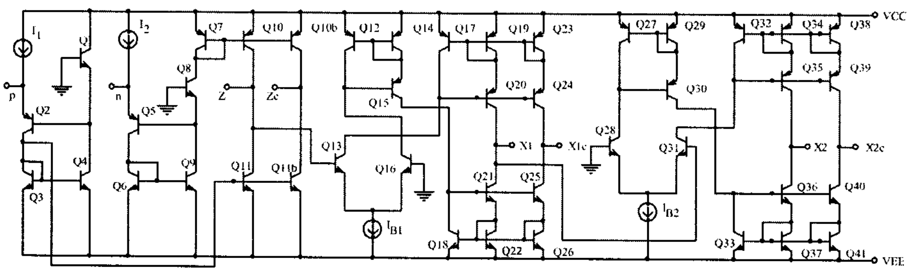

Figure 5: Bipolar design of the CDCTA.

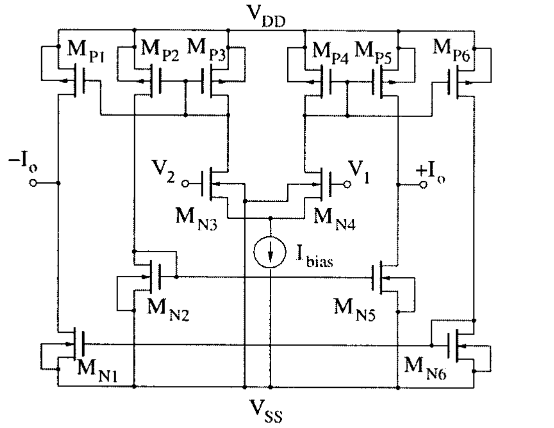

Figure 6: OTA showing one positive ($+I_o$) and one negative ($-I_o$) output.

reference to propose a new design using only two three-output OTAs.

In our proposed OTA realization of the MSO, we do not use current-differencing units [15]. We use only two three-output OTAs that can be generated by augmenting the current outputs using CMs, which can be designed as already shown in [18]. In this manner, our proposed first-order all-pass section does not require the DO-CM needed in Figure 5. We use the OTA shown in Figure 6 [19], whose outputs ($+I_o$ or $-I_o$) are augmented (mirrored [18]) to provide directly the required outputs like z, z_c, or x_{1c}, x_2, and x_{2c}.

Our proposed OTA-based all-pass section is shown in Figure 7. It consists of two three-output OTAs, one grounded capacitor, and one grounded resistor, making it suitable for whole IC design [16]. The two inputs I_{in1} and I_{in2} are connected to the outputs I_{o1} and I_{o2}, respectively, of the next section when implementing the MSO shown in Figure 2. The other I_{o3} is used to measure the phase output. In this manner, just mirroring +Io in Figure 6 directly provides the output. The analytical expression of our proposed OTA-based all-pass section is obtained as follows: The three outputs of OTA2 in Figure 7 are the same, as well as the three

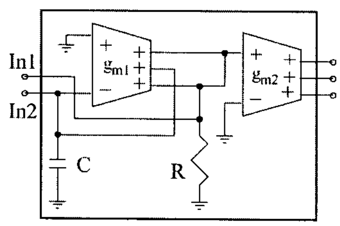

Figure 7: Proposed design of the all-pass filter using two three-output OTAs, one grounded capacitor, and one grounded resistor.

outputs of OTA1. Then: I_{in1} and I_{in2} are also the same, as: $I_{\text{in1}} = I_{\text{in2}} = I_{o1} = g_{m2}V_R$. The capacitor C is charged to generate $V_C = (I_{\text{in2}} - I_{gm1})/sC$, where: $I_{gm1} = g_{m1}V_C$, $V_R = [I_{\text{in1}} - (2g_{m1}I_{\text{in1}})/(g_{m1} + sC)]$, and $I_{o1} = I_{o2} = I_{o3} = g_{m2}V_R$, so that at the end:

$$\frac{I_{o1}}{I_{\text{in1}}} = g_{m2}R\left(\frac{s\frac{C}{g_{m1}} - 1}{s\frac{C}{g_{m1}} + 1}\right) \tag{15}$$

The expression in Eq. (15) is the one required in Figure 2. As expected, the CO and FO are also given by Eqs. (11) and (12), respectively. This expression should be negative for the last block in Figure 2. This is easily provided if the input of OTA2 in Figure 7 is connected to the negative input terminal, instead of the positive input terminal. Recall that this is needed when generating even number of phases.

Analogous to Figure 4, in our proposed OTA-based realization, in all blocks in Figure 2 the first OTA embedding g_{m1} is augmented to provide I_{-x1} and the two I_{-x1c} terminals that are required in Figure 3. As a result, using Figure 6 and augmenting its outputs just by mirroring the corresponding metal-oxide-semiconductor field-effect-transistors (MOSFETs) [18], our proposed OTA realization for the all-pass section required in Figure 2, is shown in Figure 7.

As mentioned in [20], a circuit using MOSFETs, as the OTA shown in Figure 6, should have all transistors operating in the desired region, in our case in saturation regime. To guarantee the best performance, one should optimize the IC design [21]. In this manner, we applied the optimization approach introduced in [22], to guarantee low sensitivity and then low parameter variation of the OTA. In this manner, using IC fabrication technology of 0.35 μm, and biases of $\pm$1.5 V and $I_{\text{bias}} = 50\ \mu$A, the optimized widths (W) and lengths (L) of the MOSFETs computed by applying [22] are the following: $L = 1.2\ \mu$m for all MOSFETs, $W_{\text{MP1}} = W_{\text{MP5}}$ = 72.9 μm, $W_{\text{MP2}} = W_{\text{MP3}} = W_{\text{MP4}} = W_{\text{MP6}} = 4.4\ \mu$m, $W_{\text{MN1}} = W_{\text{MN5}} = 691\ \mu$m, $W_{\text{MN2}} = W_{\text{MN6}} = 34\ \mu$m, and $W_{\text{MN3}} = W_{\text{MN4}} = 71\ \mu$m. The transconductance of the optimized OTA is shown in Figure 8 and it is equal to $g_m = 0.01\ I/V$. This design has low offset to minimize the total harmonic distortion (THD), as shown in the following section.

5. SPICE SIMULATION RESULTS

This section presents the results of the MSO design using the CDCTA and OTA realizations.

Using the CDTA shown in Figure 5, an odd three-phase sinusoidal oscillator ($n = 3$) was simulated using: $I_{B1} =$

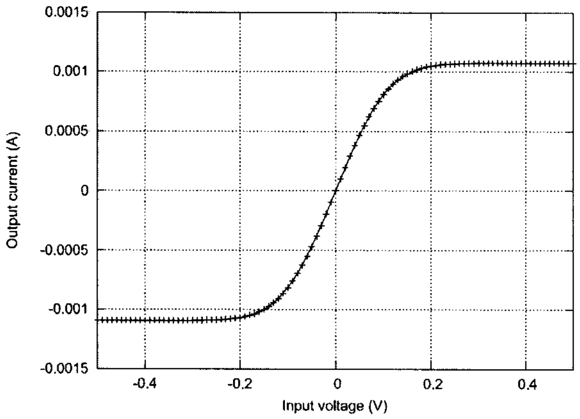

Figure 8: Transconductance of the optimized OTA shown in Figure 6.

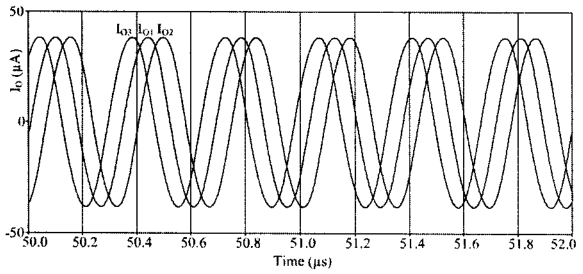

Figure 9: Current outputs of the proposed MSO using CDCTAs ($n = 3$).

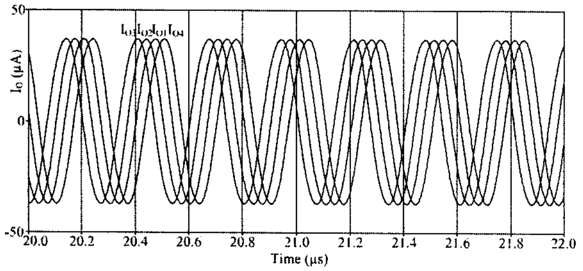

Figure 10: Current outputs of the proposed MSO using CDCTAs ($n = 4$).

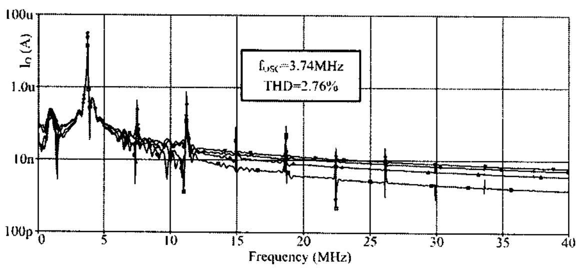

Figure 11: Spectrum of current outputs of the MSO using CDCTAs ($n = 4$).

Table 1: Tuning C and R for different values of n and FO

n	FO	C	R
2	583 kHz	2.2 nF	110 Ω
3	494 kHz	4.7 nF	120 Ω
3	957 kHz	2.2 nF	108 Ω
3	5.26 MHz	170 pF	72 Ω
4	1.21 MHz	2.2 nF	108 Ω
5	1.40 MHz	2.2 nF	108 Ω

100 μA, $I_{B2} = 62$ μA, $C = 0.1$ nF, and $R = 1$ kΩ. The output waveforms; I_{o1}, I_{o2}, and I_{o3} are shown in Figure 9, where FO = 2.93 MHz. The frequency spectrum analysis provided a THD of 2.88%. Also, an even four-phase sinusoidal oscillator ($n = 4$) was simulated by using: $I_{B1} = 110$ μA, $I_{B2} = 62$ μA, $C = 0.1$ nF, and $R = 1$ kΩ. The outputs I_{o1}, I_{o2}, I_{o3}, and I_{o4} are shown in Figure 10, where FO = 3.74 MHz. The frequency spectra of the output currents are shown in Figure 11, where the THD is 2.76%.

Using our proposed topology for the all-pass sections consisting of cascaded OTAs and shown in Figure 7, we performed simulations from $n = 2$ to $n = 5$ and for different frequencies. As the parasitic capacitances and resistances of the MOSFETs vary according to the frequency of operation, the value of R and C in Figure 7 is tuned as listed in Table 1. Also, the transconductance of the OTA can be tuned by varying I_{bias} in Figure 6. That way, the current outputs for implementing an MSO with 2–5 phases are shown in Figures 12–17.

The frequency spectrum analysis for our proposed OTA realization shown in Figure 7 provided a THD quite similar as the design using the CDCTA from Figure 5. In this manner, the computed THD for $n = 3$ for Figure 13 is 3.48%, for Figure 14 it is 3.22% and the THD for Figure 15 is 3.52%, as shown in Figure 18.

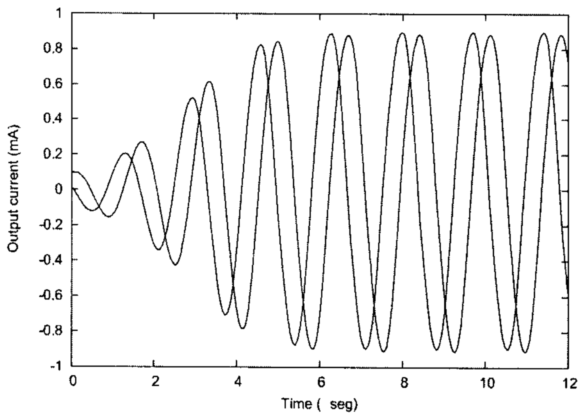

Figure 12: Current outputs using OTAs with $n = 2$ in Table 1.

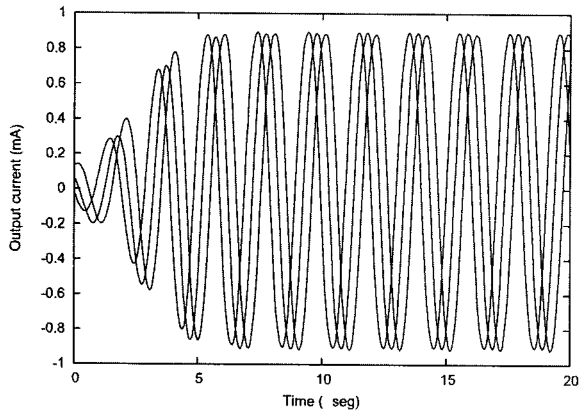

Figure 13: Current outputs using OTAs with n = 3 and FO = 494 kHz.

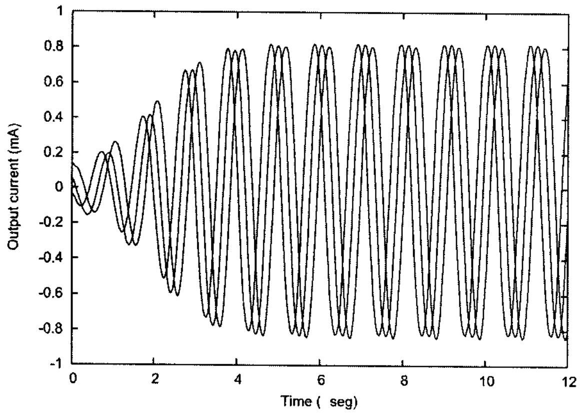

Figure 14: Current outputs using OTAs with n = 3 and FO = 957 kHz.

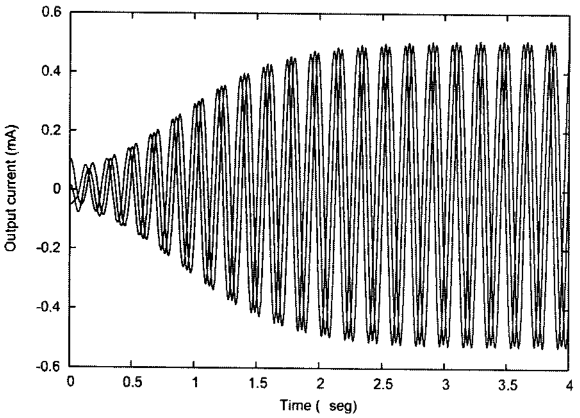

Figure 15: Current outputs using OTAs with n = 3 and FO = 5.26 MHz.

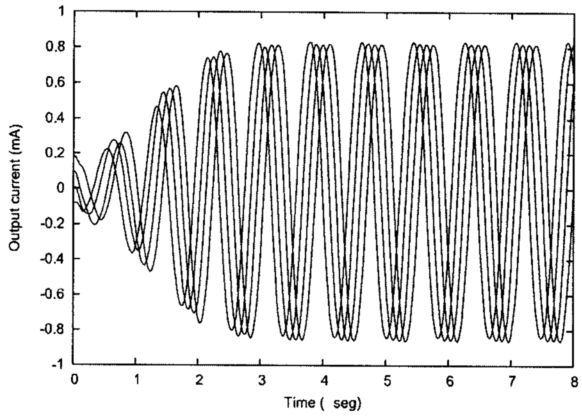

Figure 16: Current outputs using OTAs with n = 4 in Table 1.

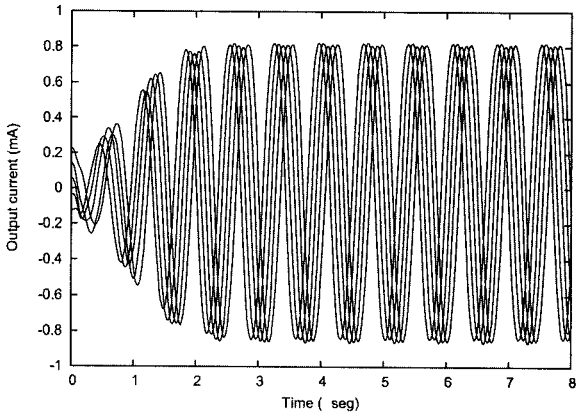

Figure 17: Current outputs using OTAs with n = 5 in Table 1.

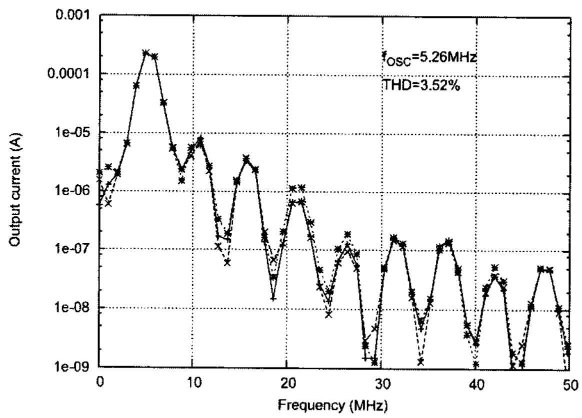

Figure 18: Spectra of the current outputs of the MSO from Figure 15.

One should recall that the design using BJTs generates all harmonics due to the exponential current characteristic of the transistor itself. However, when using MOSFETs for designing OTAs, the transistors operate in saturation region and ideally the current has a quadratic characteristic, so that the frequency spectra between the MSO designs using BJTs and MOFETs are different.

6. CONCLUSION

A new current-mode MSO topology has been introduced. It was realized using CDCTA-based first-order all-pass sections, and a reduced topology was introduced by cascading two three-output OTAs. The analytical equations for both designs and the simulations show that the FO and the CO can be independently tuned. As a result, the performance of the proposed MSO using OTAs designed with MOS IC technology of 0.35 μm showed a good generation of phases from 2 to 5 showing equal amplitude. As a final conclusion, SPICE simulations confirmed that our proposed OTA-based MSO realization is a compact one suitable for IC design.

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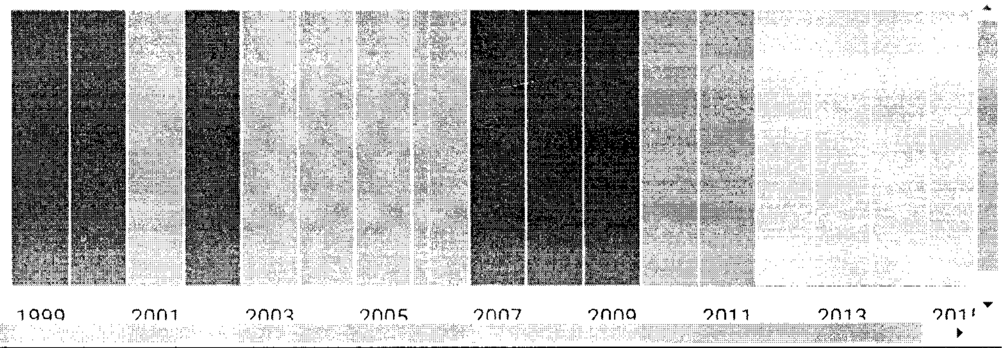

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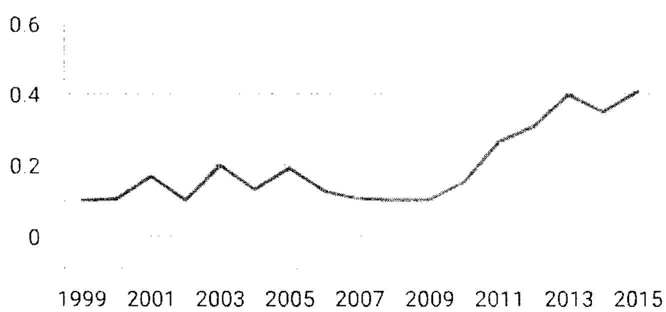

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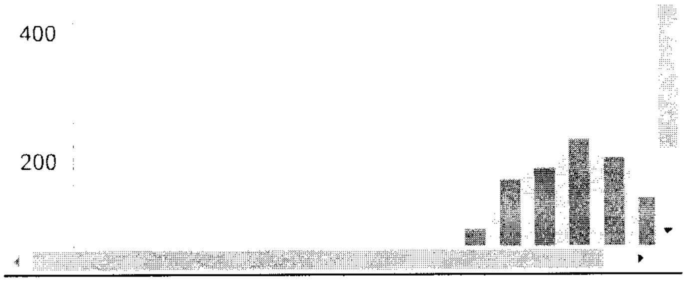

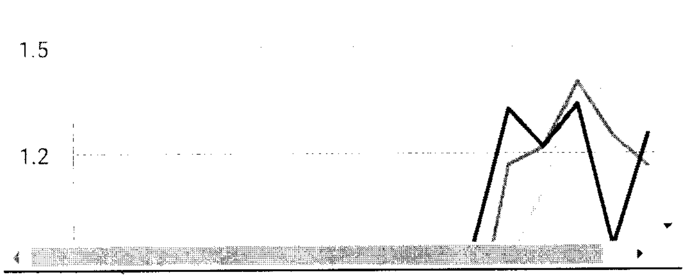

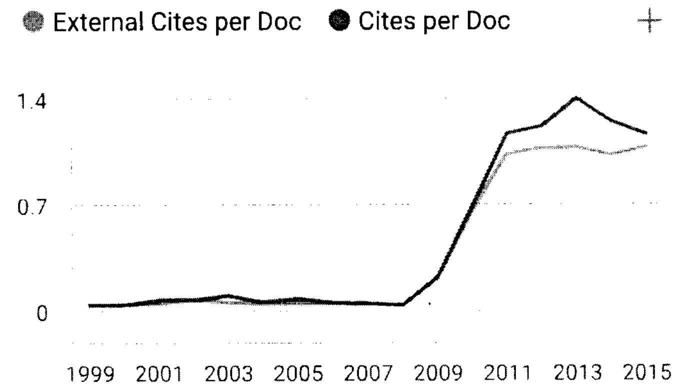

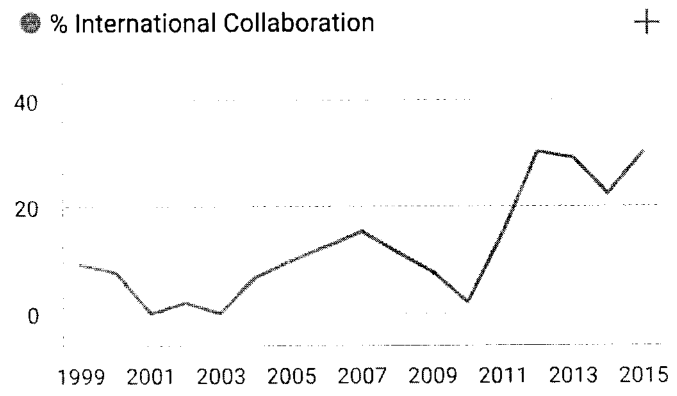

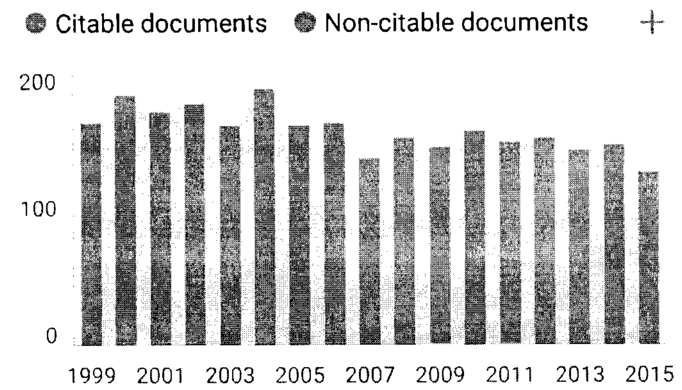

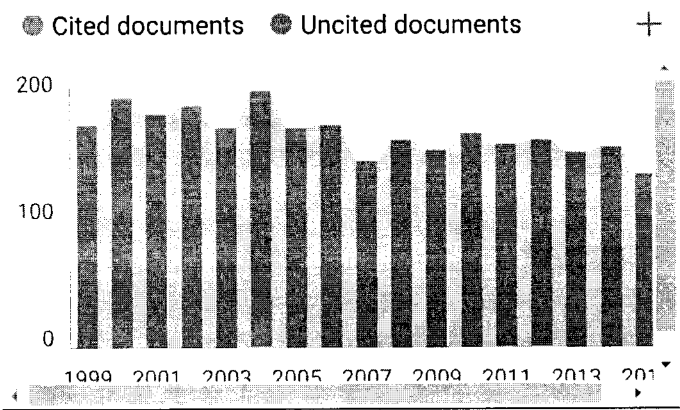

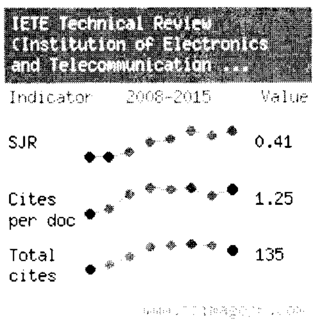

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