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PUBLICATION TYPE

Journals

ISSN

20799292

COVERAGE

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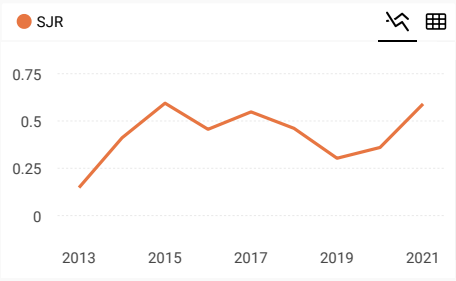

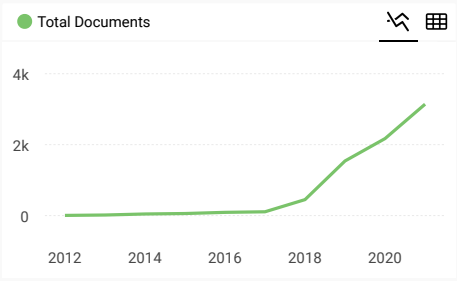

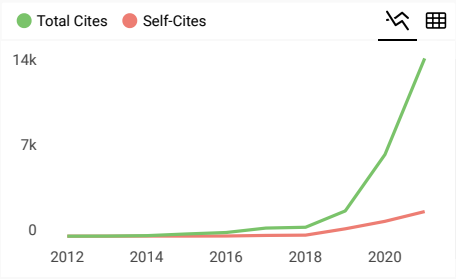

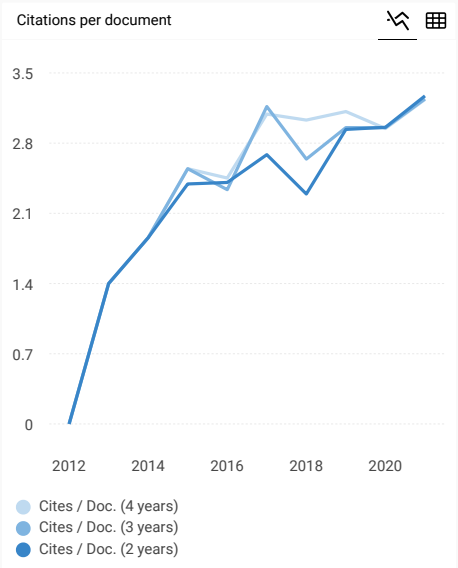

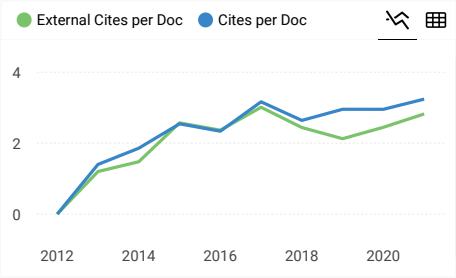

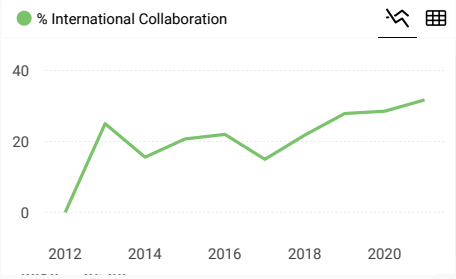

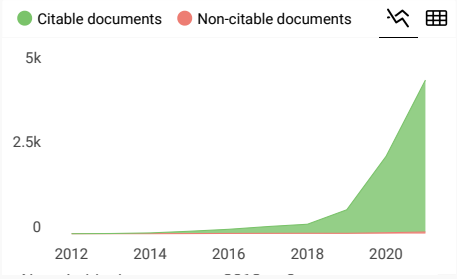

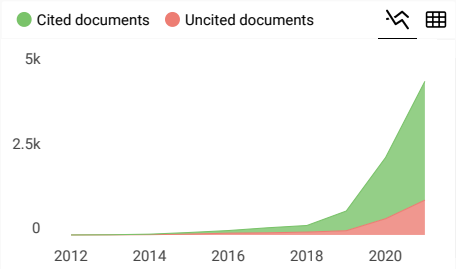

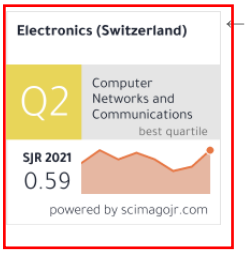

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Article

Electronically Adjustable Multiphase Sinusoidal Oscillator with High-Output Impedance at Output Current Nodes Using VDCCs

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Abstract: This paper presents the high-output-impedance current-mode multiphase sinusoidal oscillators (MSO) using voltage differencing current conveyor (VDCC)-based lossy integrators, which consist of one VDCC, one grounded capacitor, and two grounded resistors. The proposed oscillator can provide an odd-phase and even-phase system without the use of an additional amplifier. The frequency of oscillation (FO) is electronically tuned via the bias current without affecting the condition of oscillation (CO). The proposed oscillator is designed to obtain three-phase sinusoidal waveforms (n = 3). The effect of non-idealities of VDCC on the lossy integrator section is also investigated. The validity of the proposed circuit is demonstrated by PSPICE simulation using 0.18 µm TSMC CMOS process parameters with ±0.9V power supply. The frequency of oscillation obtained from the simulation is 1.43 MHz. The total harmonic distortions of the sinusoidal output currents I_{O1}, I_{O2}, and I_{O2} are 1.22%, 1.18%, and 0.57%. The I_{O1}–I_{O2} and I_{O2}–I_{O3} phase differences are approximately 121 and 119 degrees, respectively. The feasibility of the proposed MSO is also verified with experimental results using the VDCC constructed from the commercially available ICs (LT1288 and AD844) with ±5 V power supply. The results of PSPICE simulations and experiments are closely consistent with the theoretical expectation.

Keywords: high-output impedance; MSO; current mode

Citation: Pitaksuttayaprot, K.; Phanrattanachai, K.; Jaikla, W. Electronically Adjustable Multiphase Sinusoidal Oscillator with High-Output Impedance at Output Current Nodes Using VDCCs. *Electronics* **2022**, *11*, 3227. https://doi.org/10.3390/electronics11193227

Academic Editor: Sheldon Williamson

Received: 3 September 2022
Accepted: 1 October 2022
Published: 8 October 2022

1. Introduction

The multiphase sinusoidal oscillator (MSO) has received a great deal of attention in many fields, such as telecommunications, where it is used for phase-shift keying (PSK) modulation [1], measurement systems, and power electronics systems [2]. Nowadays, there is a trend of synthesizing analog signal processing circuits using active building blocks (ABB) to reduce the complexity of the circuit configuration. Using an active building block requires a minimum number of passive elements. The voltage differencing current conveyor (VDCC) is significant and well-known as an active building block, being designed for the electronic circuits in analog signal processing and emphasized by electronically controllable tuning, which provides more fine-tuning than adjusting the passive-element value in both current mode (CM) and voltage mode (VM). Attracting substantial research attention, VDCC is a versatile ABB that is reported in analog signal processing publications. It is found from the literature review that many analog circuits have been realized from the VDCC. For example, PID controller [3,4], quadrature oscillator [5–7], universal filter [8–10], first-order all-pass filter [11,12], ladder filter [13], passive element simulator [14–17], and square and triangular wave generator [18,19].

Many ABBs have been employed to realize MSOs, such as operational amplifiers (OPA) [20,21], second generation current conveyors (CCII) [22–24], second generation current-controlled conveyors (CCCII) [25], current differencing units (CDU) [26], current amplifiers (CA) [27], operational transresistance amplifiers (OTRA) [28], dual-output voltage differencing buffered amplifiers (DO-VDBA) [29], current-feedback amplifiers (CFA) [30], current differencing transconductance amplifiers (CDTA) [31,32], current differencing buffered amplifiers (CDBA) [33], voltage differencing differential difference amplifiers (VDDDA) [34], current-controlled current differencing transconductance amplifiers (CCCDTA) [35] and current-feedback operational amplifiers (CFOA) [36]. The MSO proposed in [31] requires two CDTAs per phase. In [22,28,30–33], the frequency of oscillation (FO) and the condition of oscillation (CO) are not independently controlled. The FO of the MSOs proposed in [20–24,26,28,30,32,33,36] is not electronically adjustable on the FO. The capacitors in [28,29,31,32] are not grounded capacitors. Requiring additional amplifiers [20,21,23,26,28,31,33] complicates circuits. A comparison table for the proposed MSO with other MSOs [20–36] is given in Table 1.

In this paper, the VDCC-based multiphase sinusoidal oscillator is proposed. The gain-controllable lossy integrators are used to realize the proposed multiphase sinusoidal oscillators. The lossy integrator consists of one VDCC, one grounded capacitor, and two grounded resistors. Using only one VDCC and grounded passive elements per phase is ideal for integration. The FO and the CO are independently controlled. Additionally, the frequency of oscillation is electronically tuned. Finally, the PSPICE simulation and experimental results are given to verify the performance of the proposed MSO.

Table 1. Comparison of relevant MSO.

Ref	Design Technique	ABBs	No. of Active Element per Phase	Additional Amplifier	Grounded C only	No. of R + C per Phase	Electronic Control of FO/ Simulated FO	FO and CO Independently Adjustable/Percent Error of Simulated FO	Mode of Output (CM/VM)/Simulated THD Output	Technology Used/Experiment
[20]	Lossy integrator	OPA	1	Yes	Yes	3 + 1	No/NA	Yes/NA	VM/NA	HA2544/Yes
[21]	All pass	OPA	1	Yes	Yes	3 + 1	No/NA	Yes/NA	VM/NA	LF351/Yes
[22]	Lossy integrator	CCII	1	No	Yes	3 + 1	No/NA	No/NA	VM/NA	0.35 µm CMOS/No
[23]	Lossy integrator	CCII	1	Yes	Yes	2 + 1	No/NA	No/NA	VM/NA	AD844/Yes
[24]	Lossy integrator	CCII	1	No	Yes	2 + 1	No/NA	No/NA	VM/NA	AD844AN/Yes
[25]	Lossy integrator	CCCII	1	No	Yes	0 + 2	Yes/NA	Yes/NA	CM/NA	Bipolar PR200N and NR200N/No
[26]	All pass	CDU	1	Yes	Yes	1 + 1	No	Yes	CM	OPA860/No
[27]	Lossy integrator	CA	1	No	Yes	0 + 1	Yes/0.459 MHz	Yes/12.57%	CM/1.98%	AMS CMOS 0.35 µm/No
[28]	Lossy integrator	OTRA	1	Yes	No	2 + 1	No/2.838 MHz	No/2.93%	VM/NA	AD844AN/Yes
[29]	All pass	DO-VDBA	1	No	No	0 + 1	Yes/3.5 MHz	Yes/2.77%	VM/0.78%	0.18 µm CMOS/No
[30]	Lossy integrator	CFA	1	No	*	2 + 0	No/NA	No/NA	VM/NA	AD844/Yes
[31]	All pass	CDTA	2	Yes	No	0 + 1	Yes/180 kHz	Yes/1.64%	CM/1.4%	Bipolar PR100N and NP100N/No
[32]	All pass	CDTA	1	No	No	2 + 1	No/375 kHz	No/6.25%	CM/1.032%	Bipolar PR200N and NR200N/No
[33]	Lossy integrator	CDBA	1	Yes	Yes	2 + 1	No/26.76 kHz	No/N/A	VM/N/A	AD844/No
[34]	Lossy integrator	VDDDA	1	No	Yes	2 + 1	Yes/2.5 MHz	Yes/NA	VM/0.87%, 0.86% 0.78%	TSMC CMOS technology (level 7)/No
[35]	All pass	CCCDTA	1	No	Yes	1 + 1	Yes/1.033 MHz	Yes/NA	CM/0.519%	0.25 µm TSMC CMOS technology/No
[36]	Lossy integrator	CFOA	1	No	*	2 + 0	No/NA	No/NA	VM/NA	AD844/Yes
Proposed MSO	Lossy integrator	VDCC	1	No	Yes	2 + 1	Yes/1.43 MHz	Yes/7.74%	CM/1.22%, 1.18%, 0.57%	0.18 µm TSMC CMOS technology and AD844, LT1228/Yes

* No use of external capacitor. NA: information not available/shown.

2. Principle of Operation

2.1. Basic Concept of VDCC

A voltage differencing current conveyor (VDCC) is a six-terminal active building block. The P and N voltage input terminals have high impedance, the Z current output terminal has high impedance, the X current input and voltage output terminal have low impedance, and the W_P and W_N current output terminals have high impedance. The magnitude of current at W_P and W_N terminals is the same, but they are in opposite directions. The VDCC is an active device operating both current and voltage mode systems. The electrical symbols and equivalent circuits of the VDCC are shown in Figures 1 and 2, respectively. Using the hybrid matrix form, we can describe the electrical properties of VDCC as follows [37]:

$$\begin{bmatrix} I_N \\ I_P \\ I_Z \\ V_X \\ I_{WP} \\ I_{WN} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \\ I_X \end{bmatrix}, \tag{1}$$

where g_m denotes the transconductance gain, which is controlled by the DC bias current I_B for CMOS VDCC as follows [37]:

$$g_m = \sqrt{I_B \mu_n C_{OX} W/L}, \tag{2}$$

where I_B is bias current, μ_n is the mobility of the carrier for MOS transistors, C_{OX} is the gate-oxide capacitance per unit area, W is effective channel width, and L is effective channel length, respectively. The internal construction of the CMOS VDCC employed for the realization of the proposed MSO is presented in [37].

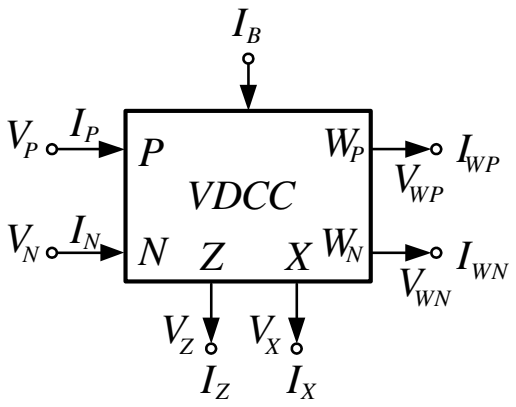


Figure 1. Circuit symbol of VDCC.

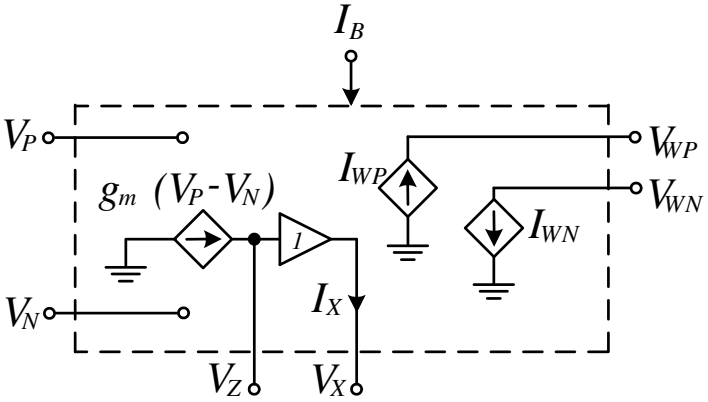


Figure 2. Equivalent circuit of VDCC.

2.2. Design of MSOs Using Lossy Integrator Circuit

The generalized structures of MSOs are realized from the principle proposed in [23,24,36], which contains the lossy integrator (first-order low-pass filter: LPF) for each phase by cascading the n identical stages ($n \geq 3$). The input of the first stage is provided by the feedback output from the nth stage, and the last section is inverted for odd-phase systems and non-inverted for even-phase systems. Each system, without any additional external amplifier, can give one phase per one lossy integrator. The system loop gain for the odd-phase system can be written as follows:

$$L(s) = \left(\frac{-k}{sa+1}\right)^n, \tag{3}$$

and the system loop gain for the even-phase system is given by:

$$L(s) = (-1)^{n-1}\left(\frac{k}{sa+1}\right)^n, \tag{4}$$

where the variable k is the voltage gain, and the variable α denotes the time constant of each integrator section. The system loop gain for the odd-phase system and even-phase system is given by:

$$L(s) = -\left(\frac{k}{sa+1}\right)^n = 1, \tag{5}$$

At oscillation frequency ($s = j\omega_{osc}$), the system loop gain is given by:

$$(j\omega_{osc}a+1)^n + (k)^n = 0, \tag{6}$$

The Barkhausen's condition of the magnitude and phase of the system loop gain are given as:

$$|L(j\omega_{osc})| = 1, \tag{7}$$

and

$$\angle L(j\omega_{osc}) = n\phi = \pi - n\tan^{-1}(\omega_{osc}a) = 2\pi, \tag{8}$$

where ϕ is the phase shift of each lossy integrator. Considering Equations (7) and (8), the frequency of oscillation (FO) and the condition of oscillation (CO) are expressed as [34–36]:

$$\text{FO}: \ \omega_{osc} = \frac{1}{a}\tan\left(\frac{\pi}{n}\right), \tag{9}$$

and

$$\text{CO}: \ k \geq \sec\left(\frac{\pi}{n}\right), \tag{10}$$

Considering Equations (9) and (10), the FO can be controlled independently of the CO by the time constant α, while the CO can be changed by the gain k without affecting the FO.

2.3. Implementation of n-Cascaded Lossy Integrator-Based Multiphase Sinusoidal Oscillator

The proposed MSO is based on lossy integrator sections, as mentioned in the preceding section. Figure 3 depicts a potential VDCC-based inverting and non-inverting lossy integrator implementation where the output voltage nodes of the inverting and non-inverting integrators are at nodes W_N and W_P, respectively. The input voltage node is high impedance. The proposed lossy integrators consist of 1 VDCC, 1 grounded capacitor, and 2 grounded resistors. The voltage transfer function of the lossy integrator is given by:

$$T(s) = \frac{V_{out}}{V_{in}} = \frac{\frac{\pm R_2}{R_1}}{s\frac{C}{g_m}+1}, \tag{11}$$

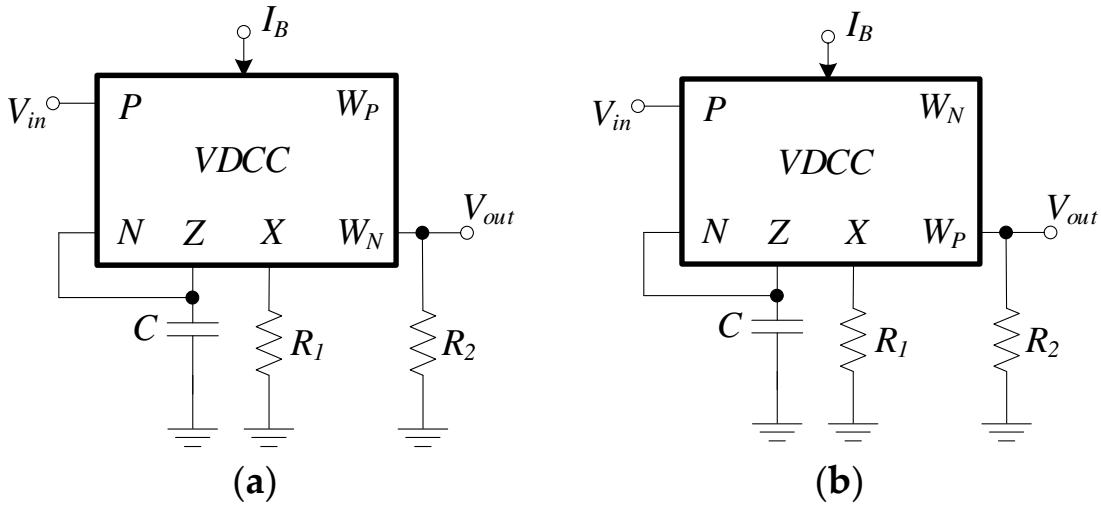


Figure 3. VDCC-based lossy integrators (**a**) inverting configuration (**b**) non-inverting configuration.

Based on Equation (3), the $k = R_2/R_1$ and $\alpha = C/g_m$. According to Equations (9) and (10), the FO and the CO are as follows:

$$\text{FO}: \ \omega_{osc} = \frac{g_m}{C}\tan\left(\frac{\pi}{n}\right), \tag{12}$$

and

$$\text{CO}: \ \frac{R_2}{R_1} \geq \sec\left(\frac{\pi}{n}\right). \tag{13}$$

Considering Equations (12) and (13), the FO can be electronically and independently tuned from the CO by the bias current I_B, while the CO can be controlled by the resistors R_1 and R_2 without affecting the FO. For amplitude stabilization, each gain-controllable lossy integrator uses a resistor R_1 that is readily constructed from a photoresistor to stabilize the output amplitude level. The 3WK16341 optocoupler with photoresistor [38] contains this component. Additional information on amplitude stabilization using 3WK16341 is provided in [39,40].

Using the identical inverting lossy integrator in Figure 3a yields the proposed odd-phase MSO shown in Figure 4. For connecting the output terminals to the load or other circuits without using an additional buffer, the output is the current (I_O) flowing out from the W_N terminal. Using the inverting lossy and non-inverting integrators in Figure 3a,b yields the proposed even-phase MSO as shown in Figure 5. Using all grounded passive elements is ideal for integration. Moreover, two grounded resistors R_1 and R_2 can be implemented from two MOS transistors [41] which will be voltage-controllable.

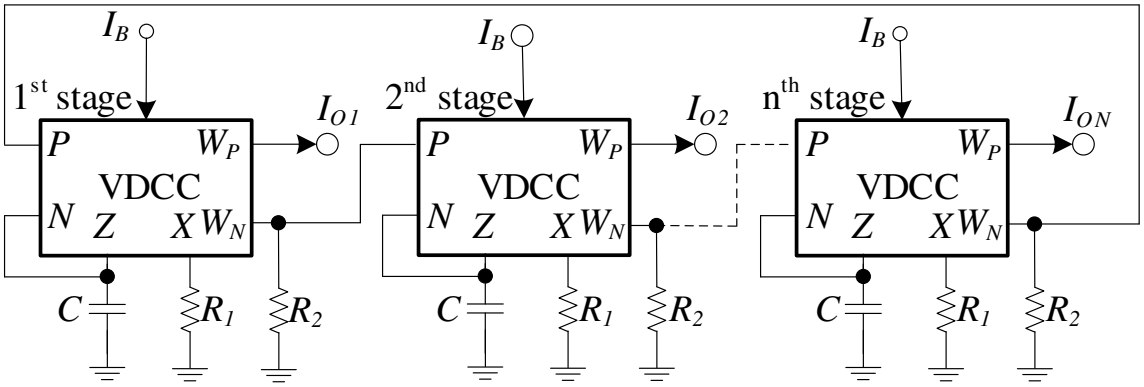


Figure 4. Proposed odd-phase MSO with high impedance at current output nodes.

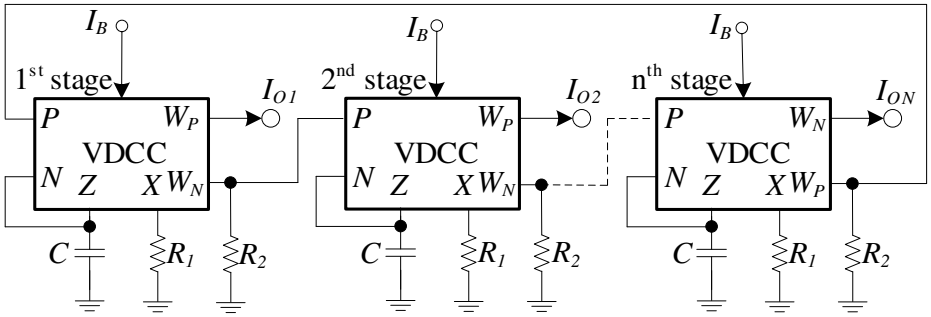


Figure 5. Proposed even-phase MSO with high impedance at current output nodes.

2.4. Non-Ideal Analysis

The effect of two non-ideal VDCC properties on the performances of the proposed MSO is studied in this section. These non-ideal cases include parasitic elements and voltage/current tracking errors. The parasitic elements of the parallel-RC impedance appearing at the high impedance input and output terminals are as follows: R_P, C_P, R_N, and C_N are at the voltage input P and N terminals, respectively; R_Z and C_Z are at the current output Z terminal; and R_{WP}, C_{WP}, R_{WN}, and C_{WN} are at the current output W_P and W_N terminals, respectively. The R_X appears in series at the low-impedance X terminal. The β parameter is the voltage tracking error from the Z terminal to the X terminal, and the α parameter is the current tracking error from the X terminal to the W_P and W_N terminal. The model of the proposed non-ideal lossy integrator circuit with parasitic elements is shown in Figure 6.

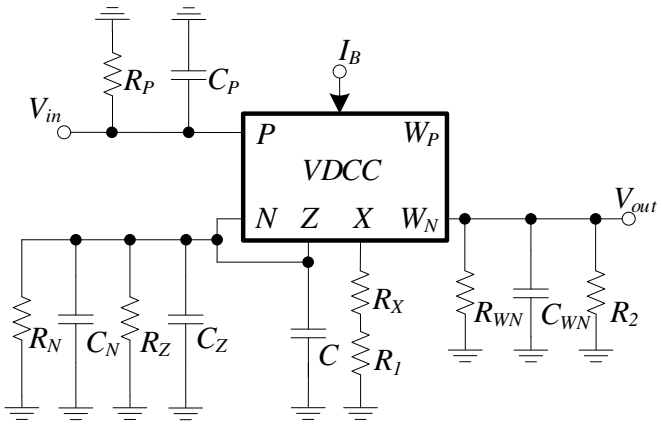


Figure 6. Model of non-ideal lossy integrator with parasitic elements.

The two-pole model [30,36] is employed to investigate the effect of the proposed non-ideal lossy integrator, which can be written in the normal form of the two-pole model as:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{-K}{\left(\frac{s}{\omega_a}+1\right)\left(\frac{s}{\omega_{p2}}+1\right)}, \tag{14}$$

where K is the voltage gain, ω_a is the dominant pole, and ω_{p2} is the second pole. Based on the circuit in Figure 6, the transfer function of the non-ideal lossy integrator can be expressed as:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{-\alpha\beta g_m \frac{R_a^* R_{p2}^*}{R_1^*}}{(R_a^* C_a^* s+1)\left(R_{p2}^* C_{p2}^* s+1\right)}, \tag{15}$$

where $R_a^* = R_N \parallel R_Z \parallel \frac{1}{g_m}$, $C_a^* = C_N + C_Z + C$, $R_{p2}^* = R_P \parallel R_{WN} \parallel R_2$, $C_{p2}^* = C_P + C_{WN}$ and $R_1^* = R_X + R_1$. Based on Equation (14), the voltage gain, the dominate pole, and the second pole can be expressed as:

$$K = \left[\frac{\alpha\beta(R_P \parallel R_{WN} \parallel R_2)}{R_X + R_1}\right]\left[\left(R_N \parallel R_Z \parallel \frac{1}{g_m}\right)g_m\right], \tag{16}$$

$$\omega_a = \frac{1}{\left(R_N \parallel R_Z \parallel \frac{1}{g_m}\right)(C_N + C_Z + C)}, \tag{17}$$

and

$$\omega_{p2} = \frac{1}{(R_P \parallel R_{WN} \parallel R_2)(C_P + C_{WN})}. \tag{18}$$

From Equation (18), the transfer function of the non-ideal lossy integrator provides an additional pole called the second pole, which is derived from the parasitic parameters. This pole mainly causes the limitation at high frequencies. According to CMOS VDCC construction, the parasitic parameters are as follows: R_P = 4.38 TΩ, C_P = 0.034 pF, R_N = 4.3875 TΩ, C_N = 0.0344 pF, R_Z = 229.426 kΩ, C_Z = 0.025 pF, R_{WP} = 186.658 kΩ, C_{WP} = 0.0105 pF, R_{WN} = 175.278 kΩ, C_{WN} = 0.022 pF. At R_2 = 2 kΩ, the frequency of the second pole is approximately 1.44 GHz. From Equation (18), R_2 should be set to a low value to enhance the second pole's frequency. If the ω_{p2} is much higher than ω_a ($\omega_{p2} >> \omega_a$), the second pole has a slight effect on the performance of the proposed MSO system. Therefore, the Barkhausen criterion yields the FO and the CO as:

$$\omega_{osc} = \frac{1}{\left(R_N \parallel R_Z \parallel \frac{1}{g_m}\right)(C_N + C_Z + C)} \tan\left(\frac{\pi}{n}\right), \tag{19}$$

and

$$\alpha\beta g_m\left(R_N \parallel R_Z \parallel \frac{1}{g_m}\right)\left(\frac{R_P \parallel R_{WN} \parallel R_2}{R_X + R_1}\right) \geq \sec\left(\frac{\pi}{n}\right). \tag{20}$$

It is found from Equation (19) that the affected dominant pole by the R_N, R_Z, C_N, and C_Z parasitic parameters reduces the performance of the FO. The CO is also affected by voltage/current tracking errors and parasitic elements, as shown in Equation (20). Moreover, it is found that the transconductance, g_m, will slightly affect the CO due to the parasitic resistance R_N and R_Z. The parasitic resistance R_Z can be varied by adjusting I_B.

3. Simulation Results

A PSPICE simulation simulated the proposed multiphase sinusoidal oscillator's performance with TSMC 0.18 µm CMOS process parameters [7,37]. The simulation was performed using the CMOS VDCC structure proposed in [37] with ±0.9 V power supply. The MOS aspect ratios are given in Table 2 [37]. Based on the circuit in Figure 4, the three-phase sinusoidal oscillator was designed. The three-phase sinusoidal oscillator was used to directly produce the generator magnetomotive forces [42]. The bias currents were set as I_B = 50 µA (g_m = 282 µA/V) and I_{B0} = 100 µA. The values of the passive elements were set as R_1 = 1 kΩ, R_2 = 2.05 kΩ, and C = 50 pF. The theoretical FO calculated from Equation (12) was 1.55 MHz. Figure 7a depicts the simulated transient current-output waveform, and Figure 7b shows the steady-state current-output waveform where the simulated FO is 1.43 MHz with a 7.74% error. Figure 7c shows the simulated output spectrum, with the I_{O1} having a THD of approximately 1.22%, the I_{O2} having a total THD of about 1.18%, and the I_{O3} having a THD of about 0.57%. The phase difference between I_{O1} and I_{O2} was about 121 degrees, and the phase difference between I_{O2} and I_{O3} was about 119 degrees.

Table 2. Transistor aspect ratios and component values.

Component	W/L [μm/μm]
M_1–M_4	3.6/1.8
M_5–M_6	7.2/1.8
M_7–M_8	2.4/1.8
M_9–M_{10}	3.06/0.72
M_{11}–M_{12}	9/0.72
M_{13}–M_{17}	14.4/0.72
M_{18}–M_{22}	0.72/0.72

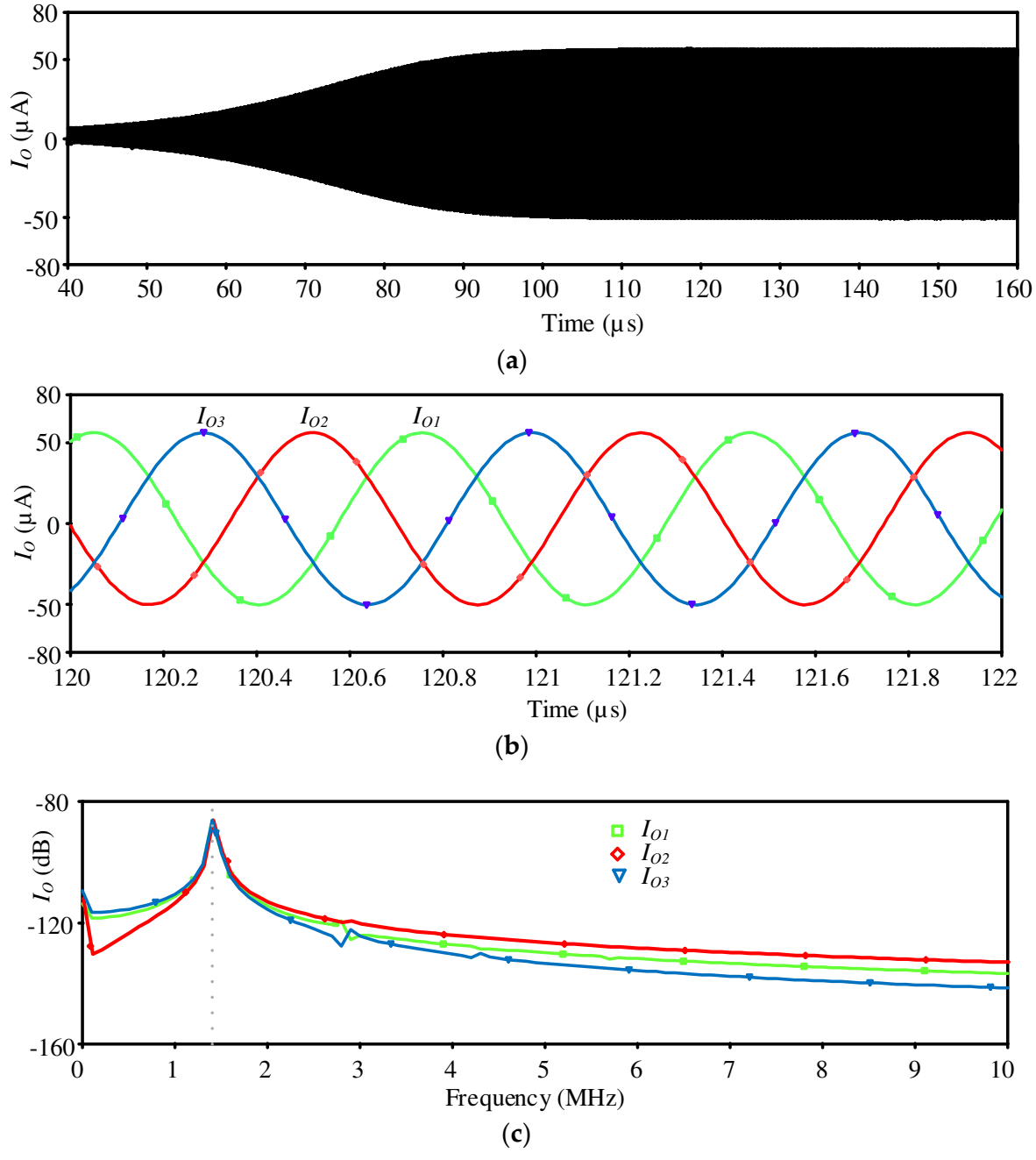
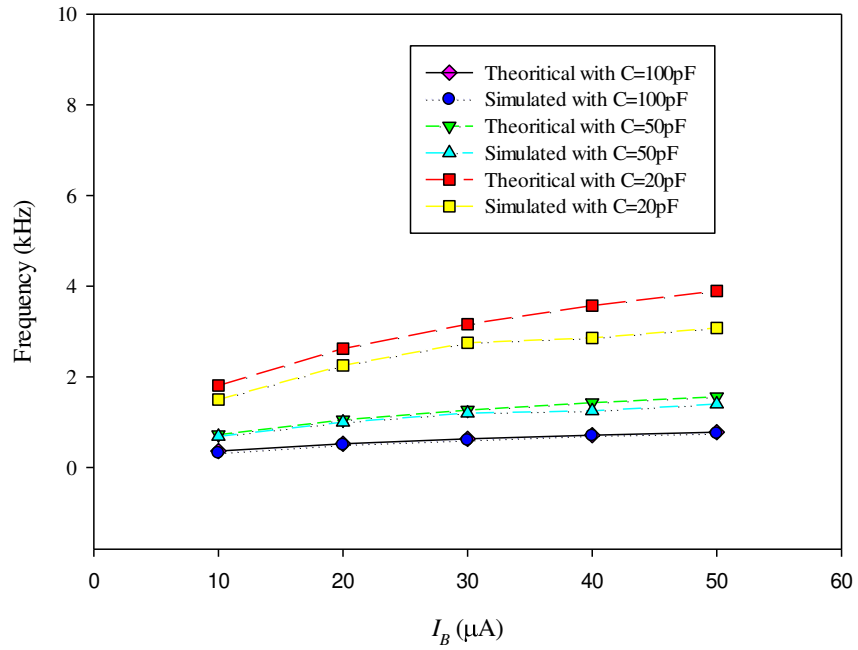
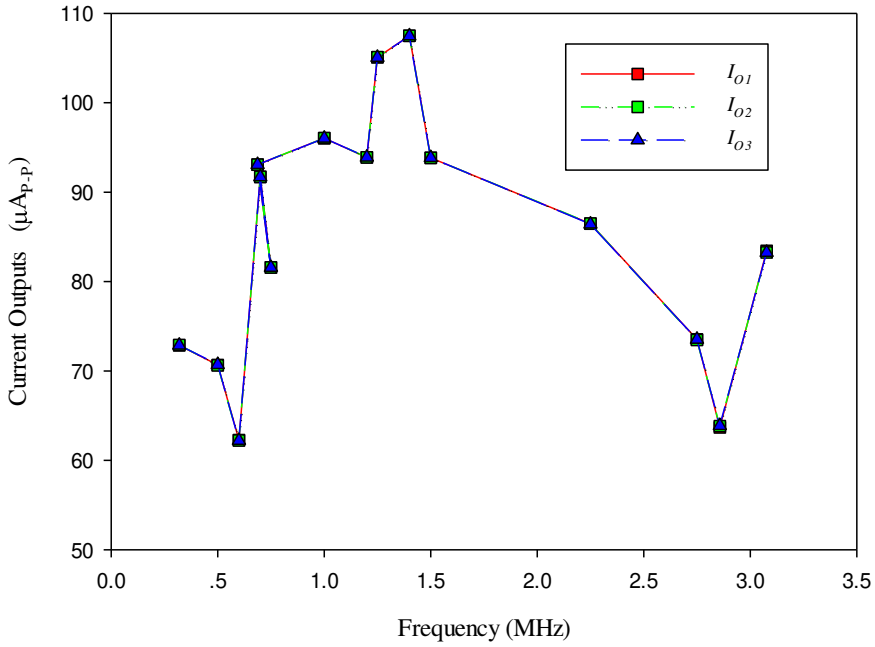


Figure 7. Simulation of the current-output waveform (**a**) initial-state (**b**) steady-state (**c**) output spectrum.

As illustrated in Figure 8a, varying the biased current (I_B) with different capacitance values yields good results of FO from the proposed MSO circuit. Figure 8b shows the magnitude of the current output waveforms during frequency tuning. The phase difference between current outputs (I_{O1} and I_{O2}) and the phase difference between current outputs (I_{O2} and I_{O3}) are depicted in Figure 8c. By adjusting the FO, the THD values in Figure 8d varied from 0.57% to 7.09%. The power consumption of the proposed circuit obtained from the simulation was approximately 2.36 mW.

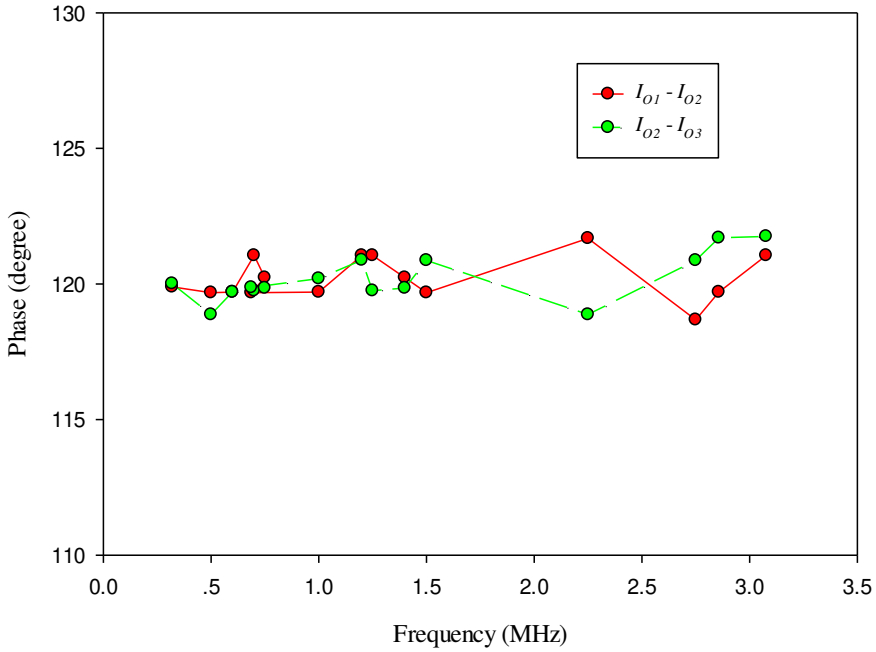


(**a**)

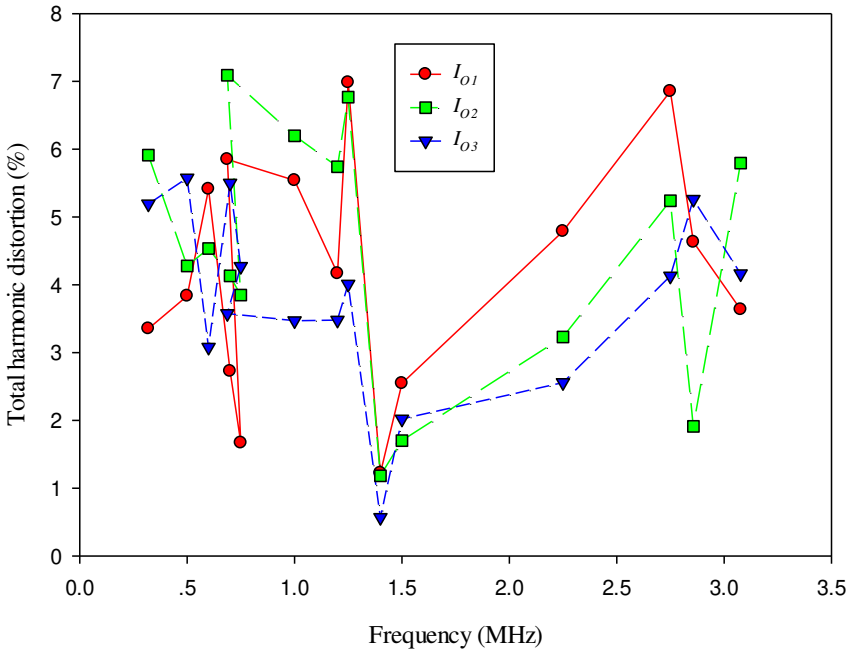


(**b**)

Figure 8. *Cont.*



(**c**)



(**d**)

Figure 8. Simulated results of (**a**) FO by varying I_B, (**b**) magnitude of current outputs, (**c**) phase difference of current outputs, (**d**) THD values of current outputs.

4. Experimental Results

For the experiment, the inverting and non-inverting lossy integrators were built up, as shown in Figure 9. The VDCC was constructed from the commercially available ICs LT1228 and AD844. For inverting the lossy integrator in Figure 9a, the resistor R_1 was connected in a floating configuration between the output of the voltage buffer in LT1228 and the X terminal of AD844. Nevertheless, all passive elements were grounded in the non-inverting lossy shown in Figure 9b. This VDCC structure contains only one W terminal. Therefore,

when the lossy integrator is constructed as the multiphase oscillator, the output waveforms for the experiment are the voltage dropped on the resistor R_2. The g_m for this construction is given as:

$$g_m = 10I_B. \tag{21}$$

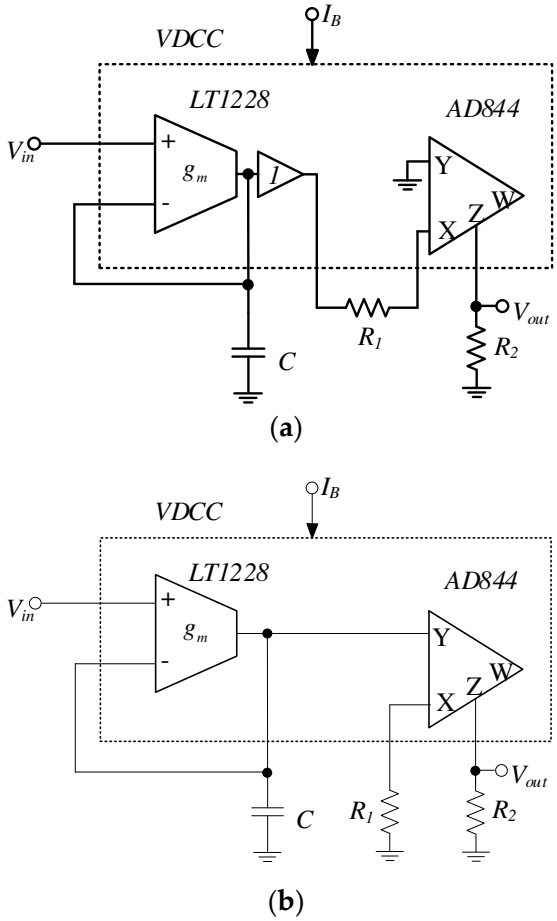
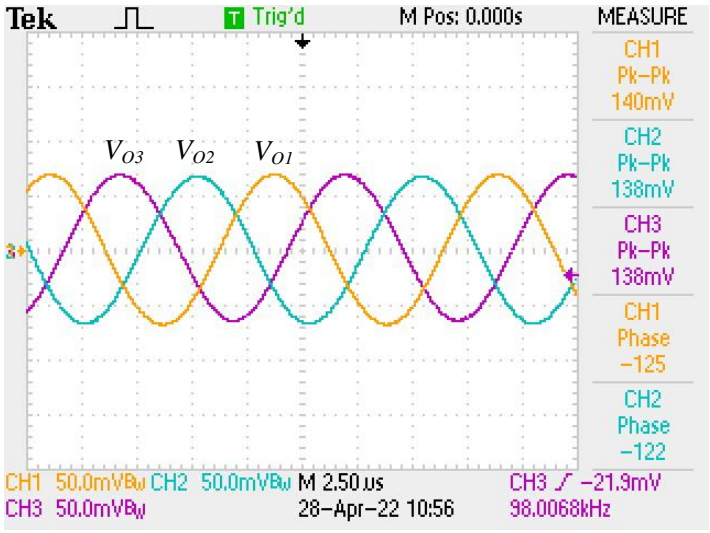


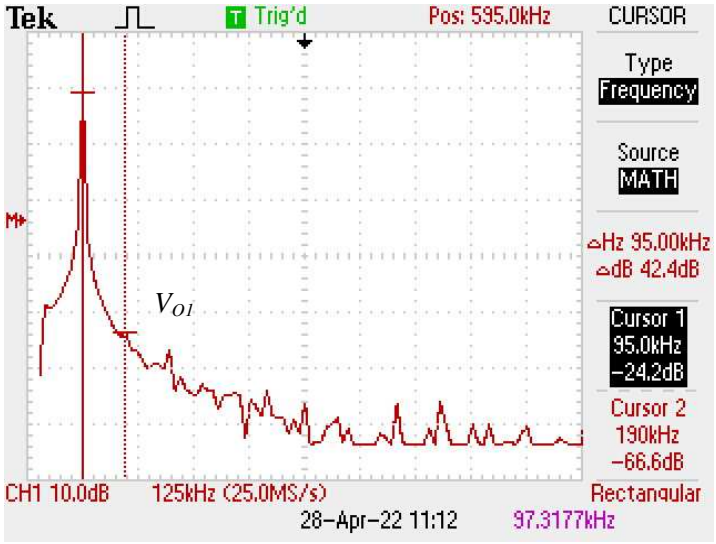
Figure 9. Commercially available ICs-based lossy integrator (**a**) inverting configuration (**b**) non-inverting configuration.

To validate the functionality of the proposed MSO, a three-phase system (n = 3) was designed using the inverting lossy integrator in Figure 9a with ±5 V power supply. The value of the bias current was set as I_B = 368 µA (g_m is 3.68 mA/V). The passive elements were chosen as R_1 = 1 kΩ, R_2 = 2.2 kΩ, and C = 10 nF. The theoretical FO calculated from Equation (12) was 101 kHz. Figure 10a shows the voltage output waveform where the experimental FO is about 95 kHz. Figure 10b, 10c and 10d show the experimental output spectrum, with the V_{O1} having a THD of approximately 0.76%, the V_{O2} having a total THD of about 1.15%, and the V_{O3} having a THD of about 1.82%.

Figure 11a shows the results of the FO by adjusting I_B with different capacitance values. The magnitudes of the voltage output waveforms in Figure 11b range from 136 $mV_{P\text{-}P}$ to 275 $mV_{P\text{-}P}$, which are similar to their magnitudes at the same frequency. As a result of maintaining the linear region operation of the operational transconductance amplifiers (OTAs), when the FO or I_B increases, all of the magnitudes tended to decrease. The phase differences of voltage outputs in Figure 11c are close to 120°. The THD values of the voltage outputs varied from 0.76% to 4.57%, as shown in Figure 11d. The power consumption of the proposed circuit obtained from the experiment was approximately 0.38 W.



(**a**)



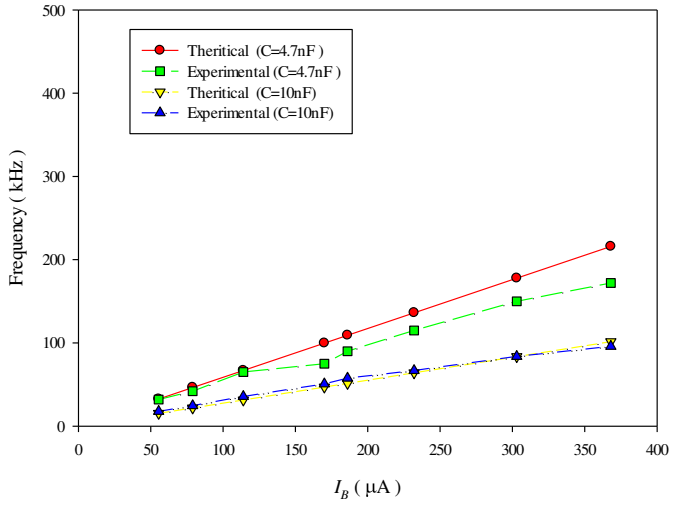
(**b**)

(**c**)

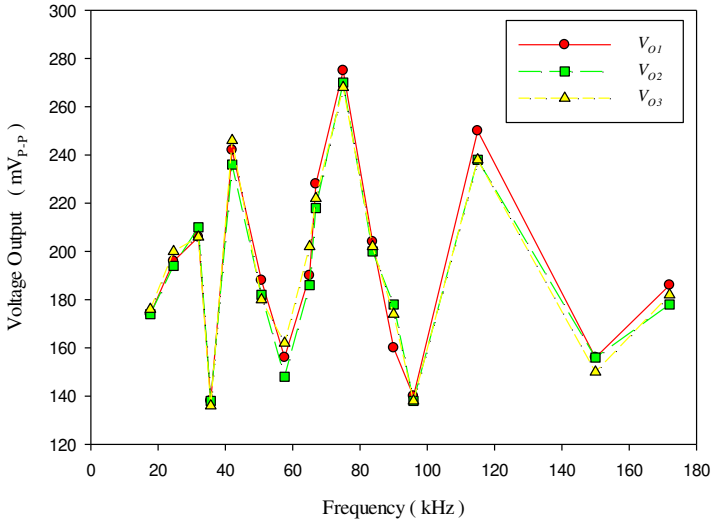
Figure 10. *Cont.*

(**d**)

Figure 10. Experimental voltage output waveforms: (**a**) three-phase sinusoidal signals; (**b**) spectrum V_{O1}; (**c**) spectrum of V_{O2}; (**d**) spectrum of V_{O3}.

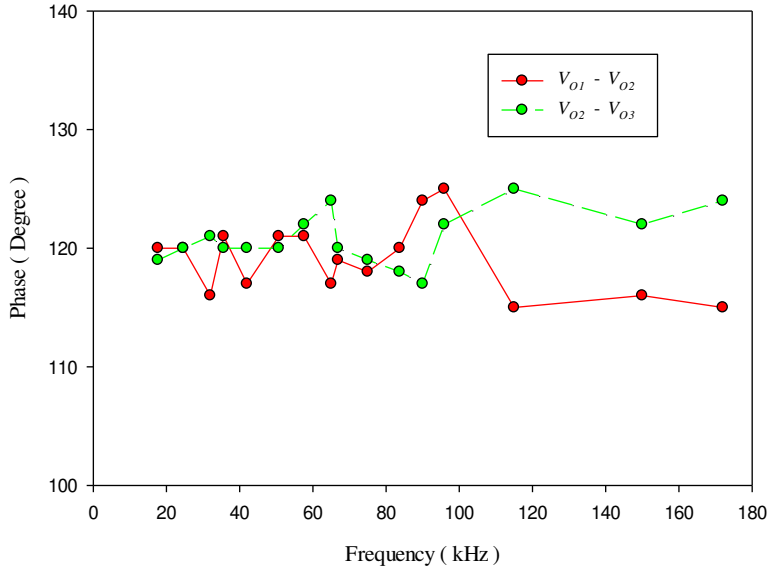


(**a**)

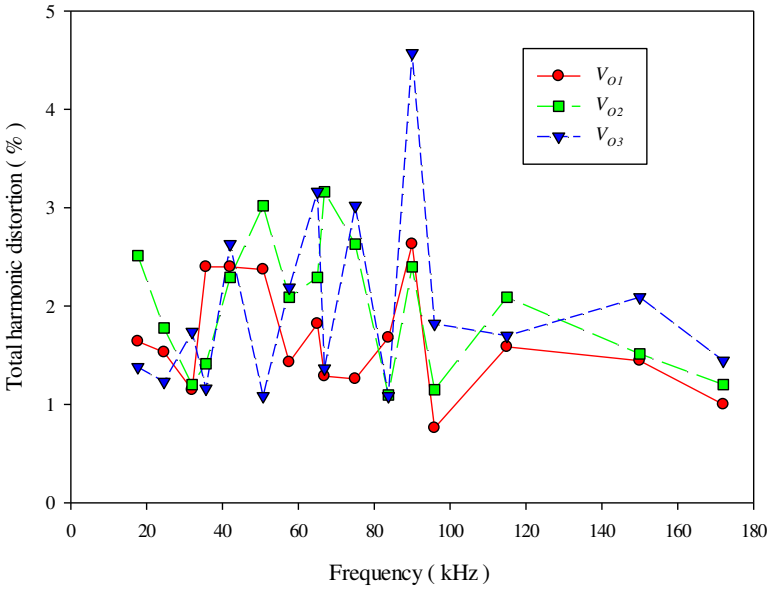


(**b**)

Figure 11. *Cont.*



(**c**)



(**d**)

Figure 11. Experimental results of (**a**) FO by varying I_B (**b**), magnitudes of voltage outputs, (**c**) phase difference of voltage outputs, (**d**) THD values of voltage outputs.

5. Conclusions

The proposed multiphase sinusoidal oscillator based on a lossy integrator structure has been presented. As it is composed of n-cascaded lossy integrators, the proposed oscillators provide even-phase or odd-phase sinusoidal waveforms without using an additional amplifier. The oscillation frequency is electronically tuned without affecting the oscillation condition. The proposed concept has been evaluated using PSPICE simulations with TSMC 0.18 µm CMOS process parameters. The simulated FO is 1.43 MHz with a 7.74% error. The THDs for $I_{O1,}$ $I_{O2,}$ and I_{O2} are 1.22%, 1.18%, and 0.57%, respectively. The phase difference between I_{O1} and I_{O2} is about 121 degrees, and the phase difference between I_{O2} and I_{O3} is about 119 degrees. The power consumption of the proposed circuit obtained from the simulation is approximately 2.36 mW. Additionally, the hardware implementation based on

the commercial ICs LT1228 and AD844 was tested. All fundamental mathematical analyses have been included, such as ideal, non-ideal, and parasitic parameters.

Author Contributions: Conceptualization, K.P. (Koson Pitaksuttayaprot) and W.J.; methodology, K.P. (Koson Pitaksuttayaprot) and W.J.; validation, K.P. (Koson Pitaksuttayaprot), W.J. and K.P. (Kritphon Phanrattanachai); formal analysis, K.P. (Koson Pitaksuttayaprot) and W.J.; investigation, K.P. (Koson Pitaksuttayaprot) and W.J.; writing—original draft preparation, K.P. (Koson Pitaksuttayaprot), W.J. and K.P. (Kritphon Phanrattanachai); writing—review and editing, K.P. (Koson Pitaksuttayaprot), W.J. and K.P. (Kritphon Phanrattanachai). All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Acknowledgments: The experiments were carried out in the Analog Circuits Design Lab of the Electronics Technology Department, Faculty of Agricultural and Industrial Technology, Phetchabun Rajabhat University, Thailand.

Conflicts of Interest: The authors declare no conflict of interest.

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